No.	*Elapsed time from start (in months) of the project*	*Milestone*	*Deliverables*	*Status*
1.	3 months	• **(Phase-1)** Completion of detailed literature review/state of the art in face recognition algorithms. • **(Phase-3)** Literature review of existing FPGA based face recognition solutions. • **(Phase-3)** Acquisition and initial testing of FPGA board • **(Phase-3)** Write and test small applications (e.g. use of camera, hard-disk, monitor interface, FPGA memory, MAC blocks, soft processors, etc) • **(Phase-4)** Literature review, market survey of existing Image enrollment and database management system.	**Phase-1** Documentation (Literature review) **Phase-3** Documentation (Literature review, acquisition and initial testing report) **Phase-3** HDL code **Phase-4** Documentation (Literature review)	Submitted Submitted Submitted Submitted
2.	6 months	• **(Phase-1)** Matlab based implementation of a standard benchmark face recognition algorithm. • **(Phase-2)** Requirement analysis for the software based face recognition application. • **(Phase-4)** Requirement analysis (finalizing the features required) in image enrollment and database management system.	**Phase-1** MATLAB code of benchmark algorithm, **Phase-2** Documentation (Requirement analysis report) **Phase-4** Documentation (Literature review, requirement analysis report)	Submitted Submitted Submitted
3.	9 months	• **(Phase-1)** Fixed point conversion of a standard face recognition algorithm. • **(Phase-1)** Evaluation and testing of the Matlab based implementation on standard databases. • **(Phase-3)** Design and implementation of non-synthesizable HDL modules of a standard benchmark face recognition algorithm implemented in matlab. • **(Phase-3)** Design and implementation of synthesizable	**Phase-1** Fixed point Matlab code. **Phase-1** Database (Standard face recognition databases) **Phase-3** Synthesizable HDL code	Pending due to funding Delay Pending due to funding Delay Pending due to funding delay

		HDL modules of standard benchmark face recognition algorithm implemented in matlab in fixed point format.		
4.	12 months	• **(Phase-2)** GUI development of a benchmark face recognition algorithm. • **(Phase-3)** Combined testing of all synthesizable HDL modules. • **(Phase-4)** Preliminary version (version-1) of Image enrollment and database management system.	**Phase-2** Software (GUI of software based face recognition application) **Phase-3** Documentation (Testing report, Test vectors) **Phase-4** Software (Image enrollment & database managment system)	Not due Not due
5.	15 months	• **(Phase-1)** Algorithm development, Investigation of approaches for multi-scale discriminant analysis. Design of a novel discriminant subband selection approach based on information theoretic analysis. • **(Phase-3)** Development of stand-alone FPGA-based real-time face recognition application (involving Camera, Hard-disk, real-time streaming issues, etc) • **(Phase-4)** Maintaining database in a hard-disk in a desired specific format which will be later used in the stand-alone FPGA-based real-time face recognition application.	**Phase-1** Documentation (Detailed report on face recognition algorithm) **Phase-3** Documentation (Detailed report on real-time FPGA based face recognition application) **Phase-4** Documentation (Format/Data-structures used for maintaining database in Hard-disk).	Not due Not due Not due
6.	18 months	• **(Phase-1)** Matlab-based implementation and optimization of the proposed algorithm. • **(Phase-3)** Extensive testing and improvement. • **(Phase-3)** Design, Implementation and testing of non-synthesizable HDL modules of the proposed face recognition algorithm	**Phase-1** Matlab code **Phase-1** Research paper(s) submitted at reputable conferences. **Phase-3** Non-synthesizable HDL code **Phase-3** Documentation	Not due Not due Not due Not due

			(Testing report, Test vectors)	
7.	21 months	• **(Phase-1)** Fixed point conversion of the algorithm. • **(Phase-1)** Evaluation and testing on standard databases • **(Phase-2)** GUI development of the proposed face recognition algorithm. • **(Phase-3)** Combined testing of all HDL modules. • **(Phase-3)** Design, Implementation and testing of synthesizable HDL modules of the proposed fixed point face recognition algorithm. • **(Phase-4)** Final version (version-2) of Image enrollment and database management system.	**Phase-1** Documentation (Evaluation, testing and comparison results on standard databases) **Phase-2** Software (Final Software-based face recongition application) **Phase-3** Synthesizable HDL code **Phase-3** Documentation (Testing report, Test vectors) **Phase-4** Software (Final Image enrollment and database management system)	Not due Not due Not due Not due Not due
8.	24 months	• **(Phase-1)** Comprehensive analysis and comparison with state of the art approaches • **(Phase-1)** Fine tuning, Improvement, Optimization • **(Phase-1)** Final documentation • **(Phase-2)** Extensive testing, optimization, and improvement. End user manual. • **(Phase-2)** Final documentation • **(Phase-3)** Integration and testing of the proposed algorithm in stand-alone FPGA-based real-time application • **(Phase-3)** Final documentation • **(Phase-4)** Extensive testing, optimization, and improvement. End user manual • **(Phase-4)** Final documentation	**Phase-1,2,3,4** Final documentation and user manual **Phase-1** Final matlab based code **Phase-3** Final HDL code **Phase-1,3** Quality Assurance report **Phase-3** Complete demonstration of the face recognition algorithm on FPGA.	Not due Not due Not due Not due Not due